CMOS Inverter Delay Simulation with parasitic elements and variation

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Inverter delay changes 50% with temperature (-10C, 85C), supply voltage and threshold voltage variation of 10%.

Abstract: For integrated circuits simulation ensures functionality. There can be variations in operating voltage, temperature and manufacturing process. During manufacturing the transistor length and the threshold voltage can vary. This report investigates propagation delay variations and shows a propagation delay ratio of 2 between a fast case with high voltage, low temperature and low Vth and a median propagation delay of 220 ps and a slow case giving a median propagation delay of 310ps.

# Introduction (Task)

Dynamic simulation of a CMOS inverter shows limitations of a given technology and confirms the correct application of a transistor model in LTSPICE simulation. The delay varies over switching cases and with load, parasitics, operating voltage, temperature and transistor threshold voltage. All these parameters were varied in simulation and delay times were extracted automatically and summarized in a box plot to show impact on delay [1]. The schematic of the circuit is shown in figure 1.



Figure 1: Inverter chain schematic

Realistic delay times can only be extracted with a realistic driver and realistic load of an inverter. There is a 1x and 5x inverter present with different drive strength and input capacitance. Additional a polysilicon line is inserted between stages having an additional RC load. The layout is shown in figure 2.

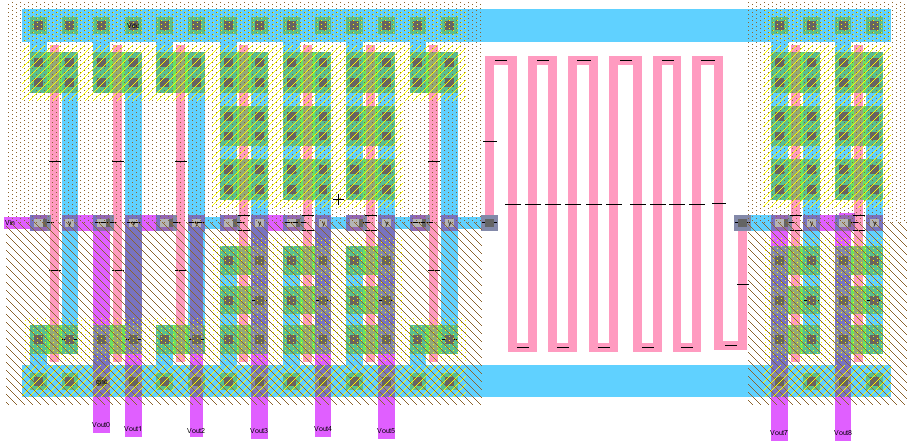


Figure 2: Inverter chain layout

The standard cells with VDD on top and GND at the bottom are used. Larger inverters are built using unit transistors in parallel or in series. The output signals are routed with the vertical pink lines in metal 2. A serpentine orange line is an added polysilicon RC delay. 4 transistor models are provided for low Vth and high Vth for NFET and PFET (LL, HL, LH, LL).

# Measurement (ACTION)

The inverter chain simulation gives the delay of rising and falling edges at all 8 outputs. Automatical measurements were implemented using the measurement statement.

.MEAS TRAN T1\_V0650 WHEN V(vout6)=V(VDD)/2 RISE=1

.MEAS TRAN T2\_V0790 WHEN V(vout7)=V(VDD)/2 FALL=1

.MEAS TRAN PROP PARAM T2\_V0750-T2\_V0650

Transistor threshold voltage, supply voltage and temperature were varied in 8 LTSPICE simulation. Each simulation gave 16 values for 8 outputs and rising and falling edges. This investigation is not possible without automation of extracting delays from simulation data. It would be convenient if the 8 LTSPICE simulations with could also be automated. The data was post processed in Excel. A template for a box plot was provided and the meaning of the the information of the box is given in figure 3.

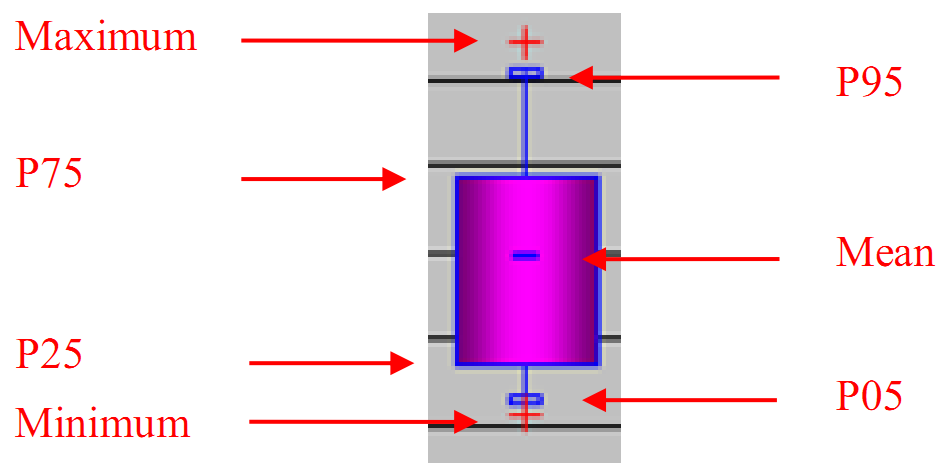


Figure 3: Explanation of the graphical information

The mean value and 5, 25, 75 and 95 percentiles can be seen in the box. A 75 percentile is drawn were 75 percent of values are below this measurement value.

The final result is shown in the figure at the top. The nominal value of delay time is around 220 ps. High temperature, low voltage or high threshold voltages increase the median values up to 320 ps.

1. Simulation Cases

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Parameter** | ***N*** | ***NV*** | ***HV*** | ***LV*** | ***HT*** | ***LT*** | ***HH*** | ***LL*** |
| VDD [V] | 1 | 1 | 1.1 | 0.9 | 1 | 1 | 1 | 1 |
| Temp [°C] | 25 | 25 | 25 | 25 | 90 | -10 | 25 | 25 |
| Vthn [V] | 0.2 | 0.21 | 0.21 | 0.21 | 0.21 | 0.21 | 0.28 | 0.14 |
| Vthp [V] | 0.2 | 0.21 | 0.21 | 0.21 | 0.21 | 0.21 | -0.28 | -0.14 |
| tDelay [ps] | 220 | 250 | 220 | 280 | 260 | 250 | 320 | 180 |

# Summary (Results and LEARNING OUTCOME)

The laboratory could be concluded in 2 laboratory sessions and 2h additional work writing this report. The importance of automation and extensive simulations was seen. A better understanding of relationship of delay, supply voltage, temperature and threshold voltage was gained.

##### References

1. Laboratory 05 Microelectronics, Joerg Vollrath, https://personalpages.hs-kempten.de/~vollratj/Microelectronics/2016\_04\_20\_Micro\_Lab05\_Parasitics\_Variations.html

Dr. Ing. Joerg E. Vollrath received 1989 his Dipl. Ing. and 1994 his Ph. D. in electrical engineering, semiconductor technology at the University of Darmstadt, Germany. Since then he worked for the memory division of Siemens and Infineon Technologies and Qimonda in various locations in the USA and Germany. He is now a Professor for Electronics at the University of Applied Science, Kempten, Germany. His expertise and interest lies in the field of design of analog and digital circuits, programmable logic, test, characterization, yield, manufacturing and reliability. He has published 22 papers and has currently 23 patents.